What is claimed is:

1. A structure comprising a carrier foil; an electrically conductive layer on one of the major surfaces of the carrier foil; a dielectric layer located on the electrically conductive layer wherein the dielectric layer having circuitry features; and metal conductive circuitry located within the circuitry features wherein the metal conductive circuitry is substantially flush/coplanar with and surrounded by the dielectric layer.

2. The structure of claim 1 wherein the circuitry features in the dielectric layer are formed completely thru it to the conductive layer.

3. The structure of claim 1 wherein the circuitry features in the dielectric layer are formed short of the conductive layer.

4. The structure of claim 1 wherein the conductive circuitry comprised lines of about 0.5 to about 1 mil wide and being about 0.5 to about 3 mils spaced apart.

5. The structure of claim 1 wherein the metal conductive circuitry comprise copper.

6. The structure of claim 1 wherein the dielectric layer comprises an epoxy resin or polyimide resin.

7. The structure of claim 1 wherein the carrier foil comprises copper.

8. The structure of claim 1 wherein the electrically conductive layer comprises chromium.

9. The structure of claim 1 wherein the flush metal conductive circuitry is covered with gold or nickel-gold.

10. The structure of claim 1 wherein the flush metal conductive circuitry is selectively covered with gold or nickel-gold.

11. The structure of claim 10 wherein gold wire bond attach exist between gold covered circuitry and other components or circuitry features attached to the structure.

12. The structure of claim 1 wherein a cavity exist thru the dielectric layer to the electrically conductive layer wherein said cavity resides an electronic component.

13. The structure of claim 1 wherein the structure is attached to a stiffening dielectric layer.

14. A structure comprising repetitive layers of a structure of claim 1 attached together by a dielectric layer.

15. The structure of claim 14 comprising interconnects from any layer of a conductive metal circuitry to any other layer of conductive metal circuitry.

16. The structure of claim 1 comprising flush metal conductive circuitry interconnects from any via in the structure to any other via in the structure.

17. A structure comprising a dielectric base layer; a second dielectric layer containing circuitry features located upon the base dielectric layer; and metal conductive circuitry located within the circuitry features wherein the metal conductive circuitry is substantially flush/coplanar with and surrounded by the second dielectric layer.

18. A structure comprising repetitive layers of the structure of claim 17 wherein the conductive circuitry comprises lines of about 0.5 to about 1 mil wide and being about 0.5

to about 3 mils spaced apart and wherein said dielectric base layers is stiffening wherein said layers are attached together by a dielectric layer.

19. The structure of claim 17 wherein the metal conductive circuitry comprises copper.

20. The structure of claim 17 wherein the dielectric circuitry containing layer comprises an epoxy resin, polyimide resin or photoimageable dielectric.

21. The structure of claim 17 wherein the dielectric base layer comprises an epoxy resin, polyimide resin or photoimageable dielectric.

22. The structure of claim 17 wherein the flushmetal conductive circuitry is covered with gold or nickel-gold.

23. The structure of claim 22 wherein gold wire bond attach exist between gold covered circuitry and other components or circuitry features attached to the structure.

24. The structure of claim 17 wherein a cavity exist thru the dielectric layer to the metal conductive layer wherein said cavity resides an electronic component.

25. The structure of claim 17 wherein the structure is attached to a stiffening dielectric layer.

26. A structure comprising repetitive layers of the structure in claim 17 attached together by a dielectric layer.

27. The structure of claim 26 comprising interconnects from any layer of conductive metal circuitry to any other layer of conductive metal circuitry.

28. The structure of claim 26 comprising flush metal conductive circuitry interconnects from any via in the structure to any other via in the structure.

29. A structure comprising a dielectric base layer; a second dielectric layer containing circuitry features located upon the base dielectric layer; and metal conductive circuitry located within the circuitry features wherein the metal conductive circuitry is substantially flush/coplanar with and surrounded by the second dielectric layer;

wherein the conductive circuitry comprises lines of about 0.5 to about 1 mil wide and being about 0.5 to about 3 mils spaced apart and circuit features of sufficient size to permit an electronic component to be located in said structure.

30. The structure of claim 29 wherein said electronic component is an integrated circuit chip and wherein a cavity exists thru the dielectric layer to the metal conductive layer and wherein said integrated circuit chip resides in said cavity.

31. The structure claim 30 wherein the flush metal conductive circuitry is covered with gold or nickel-gold, and

wherein gold wire bond attach exists between gold covered circuitry and said integrated circuit chip.

32. A method of fabricating a structure having embedded substantially flush/coplanar circuitry features which comprises:

providing carrier foil having a top side and bottom side and an electrically conductive blanket layer on said top side;

coating the electrically conductive layer with a dielectric material;

forming circuitry features in said dielectric material; and

plating conductive metal to fill said circuitry features.

33. The method of claim 32 which further comprises planarizing the side of the structure containing said conductive metal to provide a planar surface having features of conductive metal surrounded by dielectric material.

34. The method of claim 33, which further comprises the step of plating a conductive finish metal layer onto said planar surface.

35. The method of claim 35 which further comprises blanket seeding the top surface and circuit features in the dielectric material prior to plating the conductive metal.

36. The method of claim 35 wherein the conductive metal is blanket plated in the seed layer followed by planarizing the conductive metal to provide a planar surface having features of conductive metal surrounded by dielectric material.

37. The method of claim 32 wherein the circuitry features are formed through the dielectric layer and up to the conductive layer exposes said layer.

38. The method of claim 32 wherein the circuitry features are formed in the dielectric layer and short of the conductive layer.

39. The method of claim 33 wherein plating conductive metal is plated only in the circuitry features.

40. The method of claim 8 which further comprises attaching the structure after the planarizing to a substrate or dielectric.

41. The method of claim 39 which further comprises removing the carrier foil while the conductive layer protects the conductive metal from being removed, and then removing the conductive layer.

42. The method of claim 32 which comprises removing the carrier foil while the conductive layer protects the conductive metal from being removed, and then removing the conductive layer to form a smooth surface wiring on one side and a rough surface on another side.

43. The method of claim 42, which further comprises the step of plating a conductive finish layer such as gold, nickel gold or other precious metal onto said smooth surface wiring.

44. The method of claim 42, which further comprises attaching the rough surface to a dielectric material.

45. The method of claim 44 which further comprises attaching to a substrate.

46. The method of claim 36 which comprises joining at least two structures having said embedded flush circuitry features together.

47. The method of claim 32 which further comprises blanket seeding the top surface and circuit features in the dielectric material prior to plating the conductive metal;

planarizing the side of the structure containing said conductive metal to provide a planar surface having features of conductive metal surrounded by dielectric material;

optionally joining at least two structures having said embedded flush circuitry features together;

and removing the carrier foil while the conductive layer protects the conductive metal from being removed, and then removing the conductive layer to form a smooth surface wiring on one side and a rough surface on another side.

48. The method of claim 47 wherein the circuitry features are formed through the dielectric layer and up to the conductive layer exposes said layer.

49. The method of claim 47 wherein the circuitry features are formed in the dielectric layer and short of the conductive layer.

50. The method of claim 49 which further comprises attaching photoimageable dielectric layer forming vias, blanket seeding and blanket plating a conductive metal;

selectively subtractive etching the blanket plating to form conductive interconnections.

51. The method of claim 49 which further comprises attaching photoimageable dielectric layer;

forming vias;

forming interconnection between vias;

blanket seeding and blanket plating a conductive metal; and

planarizing.

52. The method of claim 21 wherein the circuitry features are formed through the dielectric layer and up to the conductive layer exposes aid layer;

and which further comprises plating a conductive material selectively onto the underlying conductive layer;

planarizing the side of the structure containing metal to provide a planar surface having features of conductive metal surrounded by dielectric material;

optionally joining at least two structures having said embedded flush circuitry features together;

and removing the carrier foil while the conductive layer protects the conductive metal from being removed, and then removing the conductive layer to form a smooth surface wiring on one side and a rough surface on another side.

53. The method of claim 32 wherein the circuitry features are formed through the dielectric layer and up to the conductive layer exposes said layer;

and which further comprises plating a conductive material selectively onto the underlying conductive layer;

attaching the structure to a stiffener; and

removing the carrier foil while the conductive layer protects the conductive metal from being removed and then removing the conductive layer to form a smooth surface wiring on one side and a rough surface on another side.

54. The structure obtained by the process of claim 32.